Grenoble is a major, world-wide scientific center. The technical expertise and the synergy between university, research, start-up and industry contribute to its successful image especially in the semiconductor field. At 35 km from Grenoble metropole, the village of Autrans is located in the Vercors massif, surrounded by an alpine landscape. The setting is wonderful: the dense and varied forests attract the amateurs of tranquility and the walkers to the discovery of relaxing paths and traditional farms.

TOPICS

Materials, Processes & Integration

- Metallization for advanced interconnects: local interconnects, contacts, metal gates, through silicon vias, power semiconductors
- Dielectrics: porous ULK, hybrid materials, pore sealing & stuffing, MOF, patterning, cleaning, restoration, surface functionalization
- Metal or dielectric liners and diffusion barriers: etch-stop, capping
- Deposition: PVD, CVD, ALD, ELD, ECD, SAMs, reflow, e-beam
- Patterning processes and integration: double & triple patterning, advanced etching techniques, Atomic Layer Etching (ALE)
- Planarization: CMP, slurry, pad, anti-corrosion methods
- Device integration and novel architectures: local interconnects
- Silicides and germanicides
- Contacts to III-V materials: CMOS, power, LED, Laser, photonics applications
- Materials for memories and memristive devices
- 1D and 2D Nanomaterials: graphene, carbon nanotubes, nanowires, nanodots
- 2D & 3D Packaging materials and technologies

Advanced Characterization and Modeling techniques

- Analytical techniques: defect inspection, X-ray/electron tomography, spectroscopy, microscopy, scanning probe methods, atom probe tomography, correlative methods
- Reliability and failure analysis: lifetime extrapolation methodologies, chip-package interaction (CPI)
- Modeling and simulation of process steps: equipment, interconnect systems, materials properties, nanoscale devices, reliability

Applications including nanoscale

- 3D integration: COW, WOW, thinning, bonding, TSV, micro-bumps
- System-on-chip and system-in-package
- Memories devices: MRAM, FeRAM, CBRAM, PCRAM, ReRAM
- Quantum Devices
- Power Electronics / IGBTs and materials / interconnects for GaN & SiC
- MEMS/NEMS: sensors and actuators

KEY DATES

- Abstract submission deadline: November 15, 2019
- Paper notification: December 20, 2019
- Welcome Dinner: March 22, 2020
- Quantum Workshop: March 23, 2020
- MAM Conference: March 24-26, 2020

Scientific Program Committee

- F. Nemouchi (Chair) – CEA-Leti, Grenoble, France
- T. Chevolleau – CNRS-LTM, Grenoble, France
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- R. Engl – Infineon Technologies, Munich, Germany
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- R. H. Dauskardt – Stanford University, USA
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- T. Ohba – Tokyo Institute of Technology, Japan

https://mam2020.web-events.net/
Keynote:

Dr Maud Vinet, Quantum computing program manager CEA-Leti

Maud Vinet (CEA-Leti, University Grenoble Alpes, France) is currently leading the quantum computing program in Leti. Together with Tristan Meunier (CNRS) and Silvano de Franceschi (Fundamental research division from CEA), they received an ERC Synergy grant in 2018 to develop silicon based quantum computer.

She defended a PhD of Physics from University of Grenoble Alps and was hired Leti in 2001 as a CMOS integration and device engineer. From 2009 to 2013, she spent 4 years with IBM to develop Fully Depleted SOI with IBM and STMicroelectronics. In 2015, she spent 6 months with Globalfoundries in Malta, NY to launch 22FDX program.

From 2013 to 2018, she managed the Advanced CMOS integration team activities in Leti (~50 people). In 2019, she was appointed project leader for the quantum computing program in Leti.

Maud Vinet authored or co-authored about 200 papers, she owns more than 70 patents related to nanotechnology and her Google h-index is 42.

Abstract:

We have put a multidisciplinary and multi institutions team which gathers quantum physicists, integration and devices engineers, circuit designers and quantum information engineers. We want to build a quantum processor. We are aiming at delivering prototypes with a 100 qubits within 6 years and at having identified the key scientific and roadblocks for scaling up.

Quantum computing is expected to extend the high performance computing roadmap at the condition of being able to operate a large number of qubits. Si-based QC appears as a promising approach to build a quantum processor; thanks to the size of the qubits, the quality of the quantum gates and the VLSI ability to fabricate billions of closely identical objects.

The quality of Si spin qubits has improved very fast with the introduction of isotopically purified 28Si, as observed by multiple research groups. In this presentation, we will discuss the architectures to design a large scale quantum computer based on Si spin qubits and we will review the associated technological challenges and needs for material development.

Quantum Workshop confirmed speakers & Sponsors:

- Francesca Chiodi, CNRS-C2N, Orsay, France
- Thomas Sand Jespersen, Niels Borh Instituted, Copenhagen, Denmark
- Ioan Pop, Karlsruhe Institute of Technology, Karlsruhe, Germany
- Manuel Houzet, CEA Grenoble - IRIG, France
- Giordano Scappucci, TU Delft, The Netherlands

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